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PARITY MECHANISM FOR DETECTING BOTH ADDRESS AND DATA ERRORS

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This mechanism is a parity-type error-detecting mechanism for use with data storage units for detecting addressing errors as well as data errors.

For each byte of data to be stored, a parity bit is generated, the value of which is determined by the number of one bits in both the data byte and the address value in the storage address counter or register. Thus, the parity which is stored represents the combined parity of both the data and the address. At the time of read-out from storage, a further parity bit is generated which is based on the number of one bits in the read-out data byte plus the number of one bits in the address which is being supplied to the storage unit at the time of read-out. This further parity bit is then compared with the previously stored parity bit to provide an error signal if (1) the read-out data byte has an error, or if (2) the read-out data was originally stored at an address which is different from the address being supplied to the storage unit to cause the read-out.

This invention is particularly useful for serial storage devices, such as charge-coupled storage devices (CCDs) and magnetic bubble memory devices. In such cases, the data is continually circulating within the storage device and the identity of the data byte currently present at the read/write station is maintained by means of an external address counter which is stepped in synchronism with the movement of the data in the storage device. Because of stray electrical noise or some other fortuitous event, the external counter may get out of sync with respect to the data circulating in the storage device. Thereafter, when data is read out, it may not be the proper data for the read-out address which is then being supplied to the storage device. The present invention enables the occurrence of this kind of error to be detected.